Local Memory and Local Controller on the board level of Data Collection Unit demonstrator

Draft

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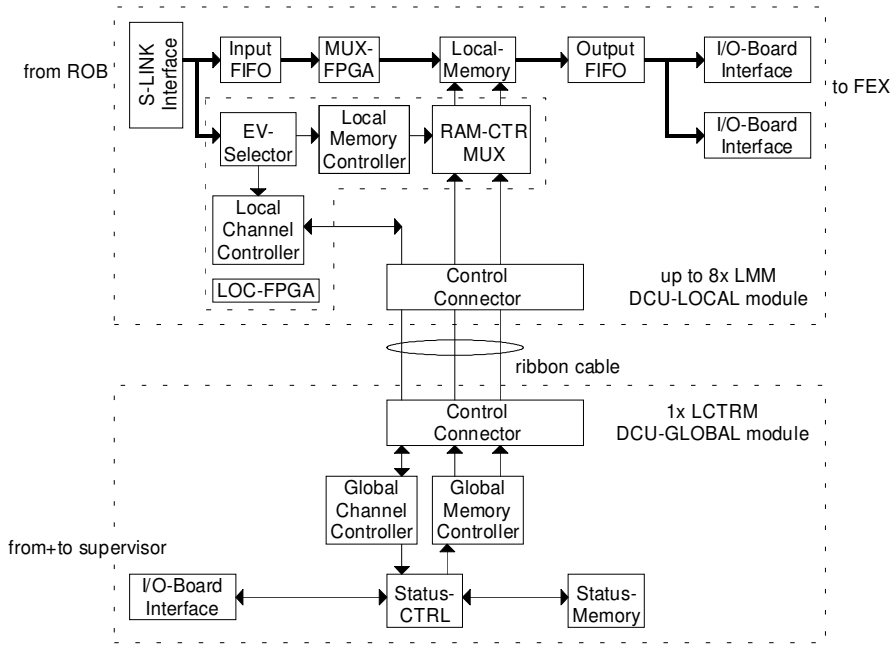
Introduction

We describe in this note the functionality of Local Memory and Local Controller on the board level of **D**ata **C**ollection **U**nit demonstrator (DCU). This description is based on EAST Note 95-02, 8. May 1995 „A Data Collection and Pre-processing Unit for the LVL2-Trigger of ATLAS“ from P. Kammel et. al. (Rev.2), graduate Informatik of A. Meister and Th. Meier and on draft designs of P. Kammel.
For the demonstrator program the DCU is scaled down to one out of the original planed 8 boards. Each of this boards should contain 8 interfaces and intelligent buffers.
The Local Memory Module is one of the intelligent buffers and the Local Controller Module is able to manage up to 8 of the Local Memory Modules.
For the demonstrator the I/O-Board from Mannheim serves as mainframe. On the I/O-Board, there are located one Local Controller Module and at least one Local Memory Module.
Originally the Local Controller, 8 Local Memories and a boardwide fast bus are the main parts located on one 9U-VME board. Now they are split in modules. The interconnection between the modules and the boardwide bus are modeled with the I/O-Board and the Backplane of ENABLE++. There is an additional ribbon cable from the Controller Module to the Memory Modules for fast access.
The task of the Local Memory Module is to extract the event information, store all incoming RoI parts from different events in the local memory and to allow the access for selective read out.
The task of the Local Controller Module is to record the incoming event number and their status. On the Local Memory Modules, distributed local memories were addressed by request from a supervisor to read out the Region of Interest (RoI) in a suitable arrangement, sorted by events and RoIs, jointed together on the boardwide bus for further processing in Feature EXtraction Processors (FEX). For the demonstrator the RoIs are jointed together in case of only one LMM on the LMM itself, in case of more than one LMM on the I/O-Board and the backplane. Furthermore the events rejected by local or global supervisor were cleared in the status memory.
The system is able to manage 1k events.



Local Memory Module

The Local Memory Module (LMM, in schematics called „DCU-LOCAL module“) consists of 3 functional main parts: the local channel controller, the local buffer controller and 2.25 MB memory. Other parts are: 36 bit input interface, input FIFO, event separator, 36 to 72 bit multiplexer, 40 pin connector to Local Controller Module, output FIFO, 2 times 36 bit output interfaces.
The Local Memory Module is designed as functional schematic, the schematic isn't ready for layout.

The **input** is a general programmable interface with 32 bit data, 4 bit status and 8 control lines and a bandwidth of 200 MB/s. The interface is programmable to handle also the S-Link specification. The data and parity supply direct the two 18 bit input FIFOs. Additional they are feed to the event separator located in the LOC-FPGA. The control lines also feed to the LOC-FPGA but the FIFOs were controlled partly from MUX-FPGA and LOC-FPGA.

Corresponding external signals:
input interface: IDATA[35:0], IF_CTRL[7:0]

Corresponding board signals:
FIFO control: WREN, WRCLK, FULL1, FULL2, RESET, RDEN, RDCLK, EMPTY1, EMPTY2

The **event separator** extracts the event information especially the event number and the event size from the data stream and informs the local channel controller and the local buffer controller located all in the LOC-FPGA.

Corresponding external signals:
input: IDATA[35:0]

The **local channel controller** (located in LOC-FPGA) is queried in a polling mode from the Local Controller Module (LCTRM, in schematics called „DCU-GLOBAL module“) to reply with the event information and a status of input interface. Every out of 8 possible LMM is queried one time in 1 µs and has 100 ns time to transfer his information. For demonstration a ribbon cable with 8 channel and 8 data lines is used for this task because the I/O-Board has no resources to allow a direct access to modular designed DCU. May be the transfer speed is to slow down for the ribbon cable connection.

Corresponding external signals:
interface to LCTRM via 40 pin ribbon cable: BUS_DATA[7:0], BUS_CHAN[7:0]

The **local buffer controller** (located in LOC-FPGA) enables the read out of an event from the input FIFOs after getting the event information and event size from the event separator. The event data are multiplexed in the MUX-FPGA to 72 bits and stored in the local memory. The event information serves as memory page address. 1k pages of 256x72 bit = 18 kbit are available. One ROB (Read Out Buffer) of endcap TRT gets in the worst case 19 kbit when every straw get a hit during all 3 bunch crossings (all pixs are black). [see R. Bock and P. LeDu, Detector and readout specifications for the level-2 trigger demonstrator program, ATLAS DAQ note 53, 15. June 1996, 3.5 Format into ROB]
The local buffer controller generates the whole signals for write operations. The signals for read out operations and refresh are generated by the LCTRM. These signals are distributed again through the ribbon cable from the LCTRM to the LMMs. If LCTRM request is pending, the local buffer controller interrupts the write operation and enables the operation with higher priority.

Corresponding external signals:
interface to LCTRM via 40 pin ribbon cable: G_ADDR[8:0], G_RAS, G_CAS, G_DTOE, G_WBWE, G_DSF, G_SCEN, G_SE, G_INT, G_GLEN, G_MASK

Corresponding board signals:
from input FIFO (IFIFO) to 36 to 72 mux (MUX-FPGA): ODATA[35:0], IDATA[35:0]
input FIFO read out enable: IMUX_RDEN
from mux (MUX-FPGA) to memory (RAM-BANK): ODATA[35:0], IDATA[35:0]
memory control parallel port: R_ADDR[8:0], R_RAS, R_CAS, R_DTOE, R_WBWE, R_DSF
memory control serial port: R_SC, R_SE, R_SE9

The **output** are two general interfaces controlled from the LOC-FPGA connected to 2 I/O-board slots. The second port of memory feeds the output FIFOs with 72 bit data. The output FIFOs are controlled mainly by MUX-FPGA. The signals MASK and MASK_OK show the availability of valid output data in the FIFOs.

Corresponding external signals:
to interface: OUTDTA[71:36], OUTDTA[35:0], SV_CTR[7:0], MASK, MASK_OK

Corresponding board signals:
from memory: ODATA[71:0], R_SC, R_SE
for OFIFO1 and OFIFO2: OFIFO_WREN, OFIFO_WRCLK, OFIFO_FULL(4:1), OFIFO_RDEN(2:1) , OFIFO_RCLK(2:1), OFIFO_EMPT(4:1), OFIFO_RESET

Local Controller Module

The Local Controller Module (LCTRM, in schematics called „DCU-GLOBAL module“) fits in one or two I/O-board slots but uses only one general interface to the mainframe. The control of the LMMs are carried out via the 40 pin ribbon cable.
The LCTRM consists of 4 functional main parts: the global channel controller, the global buffer controller, the status memory and a supervisor interface for read out requests and monitoring. All these parts except the status memory are located in only one FPGA (GLOB-FPGA).
The Local Controller Module schematic isn't designed yet but functional parts are simulated.

The **global channel controller** is polling the LMMs to get the information and status of new incoming events via the ribbon cable. The event information serves as address and the status is recorded in the status memory. The global channel controller is initialising a read out request to the global memory controller in dependence of supervisor requests and the state of a interesting event in the status memory.

Corresponding external signals:
interface to LMM via 40 pin ribbon cable: BUS_DATA[7:0], BUS_CHAN[7:0]

Corresponding board signals: DATA[15:0], ADDR[12:0], CS1, CS2, WE, OE

The **global memory controller** requests the control of the LMM memory and drives the signal sequences to initialise the read out of the local memories like a DMA cycle. But the read out of memory contents itself is performed independent of other activities. The global memory controller is able to read out single LMMs selective in any combination.
The refresh cycles are performed also like DMA access.
A very critical part is the control of the distributed memory across a ribbon cable.

Corresponding external signals:
interface to LMM via 40 pin ribbon cable: G_ADDR[8:0], G_RAS, G_CAS,
G_DTOE, G_WBWE, G_DSF,
G_SCEN[7:0], G_SE,
G_INT, G_GLEN, G_MASK

The **status memory** is organised 16 bit wide to store the status of all 8 possible channels in one word. This means that 8k location are available for event information.

Corresponding board signals: DATA[15:0], ADDR[12:0], CS1, CS2, WE, OE

The **supervisor interface** is also a general programmable interface like the input interface from LMM connected to 1 I/O-board slot. This interface receives requests from the supervisor and is able to monitor all changes of status memory.

Corresponding board signals: IDATA[21:0], IREQ, MON_DATA[23:0], MON_REQ

Corresponding external signals: DATA[35:0], EXT_CTRL[7:0]